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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/584,728	06/01/2000	Tsutomu Yoshimura	49657-700	5073

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 05/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/584,728	YOSHIMURA ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-13 and 15* is/are allowed.

6)☒ Claim(s) *4,14 and 16* is/are rejected.

7)☒ Claim(s) *17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 12/27/2004 has been entered. Claims 4-20 are pending in this Office action.

Response to Arguments

2. Applicant's arguments filed on 12/27/2004 have been fully considered but they are not persuasive.

3. Examiner's response is to address the newly added features "*a delay circuit for receiving said pulse signal and entering a meta-stable state for at least part of, but not more than, said prescribed period time" to cause delay for said prescribed period of time*". The rest of claimed limitations has been addressed in previous Office action and is recited again as shown below.

In column 1, lines 4-35, Kobayashi et al. discusses a conventional data transfer device shown in figure 1. The data transfer device formed in a semiconductor integrated circuit includes a data generating circuit 1 and a data latch circuit 2. The data generating circuit 1 receives an externally supplied transfer signal TR, and generates a data signal in response to the signal TR. The data latch circuit 2 latches the data from the data generating circuit 1 in accordance with a data latch signal DL.

Kobayashi et al. further states the problem of the conventional data transfer device shown in figure 1 in which that if a great discrepancy between timings of the

transfer signal TR and the data latch signal DL occurs due to an increase in data transfer rate, it is possible that the data latch circuit 2 does not output exact output data D_{OUT}. In other words, before the data input to the data latch circuit 2 from the data generating circuit 1 has been stabilized, a data latch signal DL may be input to the data latch circuit 2.

In recognizing the aforementioned problem, Kobayashi et al. teachings address the shortfall of the conventional data transfer device by providing a data transfer device which *precisely controls data transfer while preventing unstable* data from being latched; see column 1, lines 35-45. Kobayashi et al. implements a latch control circuit 7 as shown in figure 2A, and further shown in details in one embodiment of figure 4. As recited in previous Office action, inverters 9a, 9c, 9h, transfer gates 10a and 10b form the mask signal generating circuit which generates a low level mask signal at node N2 having a pulse width in accordance with the delay time defined by the inverter circuit 9c, see column 6 lines 17-45. Kobayashi et al. further expresses (see column 8, lines 10-21) that the mask signal at least in part determining a time delay between the transfer signal and the generation of the data latch (DL) signal. In light the foregoing discussion, the mask signal generating circuit described in the second embodiment is equivalent to the claimed pulse generator, wherein a mask signal is generated in response to input data D as shown in figure 6. Figure 5 shows outputs N3 N4 N5 N6 from the inverters 9b 9d 9g 9e effectively delay the data latch (DL) signal by a prescribed delay time determined by inverter 9c until data is stabilized. In light of the foregoing disclosure, the inverters 9b 9d 9g 9e performs an equivalent function of a delay circuit, as claimed in

the instant application, for receiving the output of the mask generating circuit and causing delay by a prescribed time delay. Hence, inverters 9b 9d 9g 9e enter a meta-stable state for at least part of, and delay data latch (DL) signal by a prescribed delay time until data is stabilized. Obviously, the meta-stable state is less than the prescribed period time due to stable data signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Kobayashi et al. U.S. Patent 5,576,643.

Regarding claim 4, admitted prior art discloses in figure 8 a conventional digital synchronous circuit including:

- a multi-phase clock generating circuit 10 for outputting n clock signals CLK1 to CLKn;
- a plurality of first latch circuits for taking in an input data signal according to corresponding ones of said plurality of clock signals;
- a plurality of second latch circuits for taking in and holding outputs of first latch circuits;

- However, admitted prior art does not show a control circuit for outputting a control signal to the second latch circuits according to a change in the input data signal. Kobayashi et al. invention discloses a data transfer circuit device including a data transfer circuit, a latch control circuit and a data latch circuit. According to one embodiment as shown in figure 2B, the data transfer circuit 6 outputs data D in response to an externally supplied transfer signal TR. The latch control circuit 7 generates *a data latch signal DL based on an externally supplied latch control signal and on a data D* supplied from the data transfer circuit 6. Kobayashi et al. further shows a latch control circuit 70 in accordance with a second embodiment of the invention, see figure 6. The latch control circuit 70 is very similar to the latch control circuit in figure 4. In figure 4, inverters 9a and 9c and the transistors Tr1 and Tr2 form a mask signal generating circuit which generates a mask signal at node N2 which set N2 low, see column 4 lines 54-62, also figure 5. In figure 6, an inverter 9h and transfer gates 10a and 10b are provided in place of the transistors Tr1 and Tr2 of the latch control circuit in figure 4. In view of that, inverters 9a, 9c, 9h, transfer gates 10a and 10b form the mask signal generating circuit which generates a low level mask signal at node N2 having a pulse width in accordance with the delay time defined by the inverter circuit 9c, see column 6 lines 17-45. Kobayashi et al. further expresses (see column 8, lines 10-21) that the mask signal at least in part determining a time delay between the transfer signal and the generation of the data latch (DL) signal. In light the

foregoing discussion, the mask signal generating circuit described in the second embodiment is equivalent to the claimed pulse generator, wherein a mask signal is generated in response to input data D as shown in figure 6. Figure 5 shows that the data latch (DL) signal does not go high when data is being switched, and goes high when the data stabilized after the delay time determined by the inverter circuit 9c. Figure 5 shows that outputs N3 N4 N5 N6 from the inverters 9b 9d 9g 9e effectively delay the data latch (DL) signal by a prescribed delay time determined by inverter 9c until data is stabilized. Hence, the inverters 9b 9d 9g 9e perform an equivalent function of a delay circuit, as claimed in the instant application, for receiving the output of the mask generating circuit and causing delay by a prescribed time delay. In light of the aforementioned discussion, the latch control circuit 70 performs equivalent function of the claimed control circuit.

- Kobayashi et al. invention provides a data transfer device, which precisely controls data transfer while preventing unstable data from being latched. Kobayashi et al. disclosure is in the same field of endeavor with the instant application. Furthermore, Kobayashi et al. teaches utilization of the latch circuit to solve the problem of indefinite state of data that the prior art encounters. Therefore, one of ordinary skill in the art would have been motivated to modify admitted prior art to include a latch control circuit, as taught by Kobayashi et al., to prevent indefinite state of data before transferring data.

- The newly added features ""*a delay circuit for receiving said pulse signal and entering a meta-stable state for at least part of, but not more than, said prescribed period time*" is already discussed in (3) above.

Regarding claim 14, admitted prior art further shows, in figure 8, a clock phase determination circuit 50 and a selector 60 that perform the same functionality as claimed in the instant application.

Regarding claim 16, as recited in claim 4, inverters 9b 9d 9g 9e perform an equivalent function of a delay circuit, as claimed in the instant application, for receiving the output of the mask generating circuit and causing delay by a prescribed time delay. Furthermore, inverters 9b 9d 9g 9e, corresponding to the claimed delay circuit, receives output N2 of the mask generating circuit, corresponding to the claimed pulse generating circuit, at a data input node, and further receives a latch control signal LC (see also figures 2A and 4), at inverter 9g, corresponding to the claimed clock input node. In light of the foregoing discussion, inverters 9b 9d 9g 9e act as a latch circuit. Therefore, a person of ordinary skill in the art would have recognized the interchangeability of the inverters 9b 9d 9g 9e taught in Kobayashi et al. invention for the corresponding third latch circuit claimed in the application claim.

Allowable Subject Matter

5. Claims 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 5-13 and 15 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 5, said claim is directed to a digital synchronous circuit wherein the digital synchronous circuit has been amended to claim uniquely distinct features "wherein said control circuit includes a first pulse generating circuit for generating a first pulse signal according to a change in said input data signal" and "a third latch circuit for receiving said first pulse signal at a data input node and a clock input node" and "a level determination circuit for outputting a detection signal when potential of an output signal from said third latch circuit has crossed a reference potential" and "a second pulse generating circuit for generating a second pulse signal according to a change in potential of said detection signal and outputting said second pulse signal as said control signal". The closest prior art, Kobayashi et al. (US Patent 5,576,643) disclosing a data transfer circuit device, either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TESFALDET BOCURE
PRIMARY EXAMINER

KCT